UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,135	04/02/2001	Anthony M. Andric	1001-0144	8930

22120 7590 08/13/2003

ZAGORIN O'BRIEN & GRAHAM LLP
401 W 15TH STREET
SUITE 870
AUSTIN, TX 78701

EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 08/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,135	ANDRIC ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-18,20,22-24,26 and 27* is/are rejected.

7)☒ Claim(s) *9,19,21,25,28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The present Office Action is responsive to Applicant's amended Response filed March 26, 2003. The Examiner acknowledges the amendment to Claim 20 and the addition of new Claims 28 and 29. Accordingly, Claims 1-29 are now pending in the instant amended Application.

Claim Objections

2. Claim 22 is objected to because of the following informalities:

In Claim 22, line 2: "respectfully" should be changed to --respectively--.

Appropriate correction is required.

Rejections Based On Prior Art

1. The following references were relied upon for the rejections hereinbelow:

Tamarkin et al. (US 6,049,467)*	Ito et al. (US 5,885,092)*
Miremadi et al. (US 5,854,507)*	Mostafazadeh et al. (US 5,783,870)*
Pecone et al. (US 5,628,637)*	Ikesugi et al. (US 5,556,286)*
Miller (US 5,130,894)*	Khosrowpour et al. (US 6,477,593 B1)*
Bolotin et al. (US 6,206,705 B1)	

*Previously made of record in the instant Application.

Claim Rej ctions - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-6, 15, 16, 18, 20, 22-24, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Tamarkin et al. in conjunction with the "package" definition of Bolotin et al.

Examiner's Note: Bolotin et al. is being used only for the purpose of providing a definition of a "package" in order to justify and support the Examiner's identification of the modular printed circuit boards 13a and 13b of Tamarkin et al. as the Applicant's claimed IC "packages." Thus, the above-captioned rejection is a multiple reference 35 USC § 102(e) rejection in accordance with MPEP § 2131.01 (see the relevant parts II and III).

As to Claim 1:

(i) Tamarkin et al. discloses, in Fig. 1, a stack of two IC packages 13a and 13b on a printed circuit board 12, and further discloses that the IC stack can be increased from two to N boards depending on the requirements of the application (col.4: 66-col.5: 5). Therefore, package 13b can be adapted to include connectors/contacts 20, identical

to the package 13a, in order to receive another package "13c" in a stack of three (or more) packages. Accordingly, the Examiner regards Fig. 1 as the disclosed embodiment stacking $N \geq 3$ packages 13 on printed circuit board 12, wherein package 13b in the stack is structurally and electrically identical to the package 13a shown in Figs. 1 and 2 (i.e., package 13b also has connectors/contacts 20). Therefore, Tamarkin et al. discloses, in Fig. 1: a first integrated circuit (IC) 24 mounted in a first package 13b, the first package 13b having *a first set of electrical contacts A, B* (within connector 20--see Figs. 4 or 5--on the upper surface of package 13b, but not shown in Fig. 1 as discussed above) and **a first connector 18** (on the lower left-hand-side surface of package 13b in Fig. 1); a second IC 24 mounted in a second package 13a, the second package 13a having *a second set of electrical contacts A, B* (within connector 20 on the upper right-hand-side surface of the package 13a in Fig. 1) and **a second connector 20** (on the upper left-hand-side surface of package 13a in Fig. 1), **the second connector 20** being electrically and physically coupled to **the first connector 18** (Fig. 1), **the first and second connectors 18 and 20** being mating connectors (col.4: 33-37 and 44-49).

(ii) Bolotin et al. teaches that modular single chip or modular multi-chip printed circuit boards are considered in the art to be a "package," as shown in the exemplary Fig. 1 and described in col.1: 25-33 and col.2: 5-13. A plurality of printed circuit board (PCB) packages 242, 246 and 400 of the type shown in Fig. 1 are stacked on yet another printed circuit board, i.e., main chassis printed circuit board 200 (Fig. 2; col.2: 14-20 and 46-59). The modular PCB packages, as shown in Fig. 1, and applied as

PCB packages 242, 246 and 400 in the stacked structure of Fig. 2, come in many types, such as memory, processor, or power module packages (col.1: 25-33). The application and modular structure of the PCB packages of Figs. 1 and 2 in Bolotin et al. are analogous to the PCB packages of Tamarkin et al., as relied upon for the rejections of Claims 1-6, 15, 16, 18, 20, 22-24, 26 and 27 under 35 USC § 102(e). The PCB packages 13a and 13b of Tamarkin et al. are, like those of Bolotin et al., also modular memory packages, each of whose respective packaging substrate is a printed circuit board (Tamarkin et al.: Figs. 1 and 2; col.4: 27-29) mounted on a main board 12 (col.4: 11-12 and 27-33).

(iii) Since both Bolotin et al. and Tamarkin et al. are directed to the formation of a three-dimensional electronic system comprising multi-chip modules stacked onto a main printed circuit board, and since Bolotin et al. teaches that each multi-chip module is, in fact, a "package" formed on a printed circuit board, then the multi-chip modules 13a and 13b that are formed on printed circuit boards in Tamarkin et al. are each as much a "package" as the multi-chip printed circuit board module taught in and defined as a "package" by Bolotin et al. Therefore, the Examiner is correct and justified in identifying the multi-chip printed circuit boards 13a and 13b of Tamarkin et al. as IC "packages," analogous to the printed circuit board modules taught and defined as "packages" by Bolotin et al.

As to Claim 2, Tamarkin et al. further discloses that *the first set of electrical contacts A, B* are disposed on a first (upper) surface of package 13b (but not shown in

Fig. 1, as discussed above) and **the first connector 18** is disposed on a second (lower) surface of package 13b (Fig. 1).

As to Claim 3, Tamarkin et al. further discloses that *the second set of electrical contacts A, B* and **the second connector 20** are disposed on a same (upper) surface of the second package 13a (Fig. 1).

As to Claim 4, Tamarkin et al. further discloses, in Figs. 1 and either of 4 or 5) that the second set of electrical contacts A, B (within connector 20 on the upper right-hand-side surface of the package 13a in Fig. 1) are coupled to a printed circuit board 12 through **an** intermediate connector 18 (Fig. 4 or 5) on the lower right-hand-side surface of package 13a in Fig. 1 (and therethrough to **another** intermediate connector 20 and, thereby, to board 12 in Fig. 1).

As to Claim 5, Tamarkin et al. further discloses that the intermediate connector 18 is a socket (Fig. 2).

As to Claim 6, Tamarkin et al. further discloses that first and second connectors 18 and 20 are male/female connectors (col.4: 33-37).

As to Claim 15, Tamarkin et al. discloses, in Fig. 1: electrically coupling a first integrated circuit (IC) 24 mounted in a first package 13a through a first set of electrical connectors 18 to a printed circuit board 12; electrically connecting the first IC 24 through a first package connector 20 to a second IC 24 mounted in a second package 13b having a second package connector 18 (Fig. 1 and either of Figs. 4 or 5; col.4: 34-46), wherein the first and second package connectors 20 and 18, respectively, are mating connectors (col.4: 33-37).

As to Claim 16, Tamarkin et al. further discloses that the second package 13b is coupled to printed circuit board 12 by way of connectors 18 and 20 on first package 13a and connector 20 on printed circuit board 12.

As to Claim 18, Tamarkin et al. further discloses that the second package connector 18 is electrically connected to the first package connector 20 via a mechanical (i.e., solderless) male/female connector mating (col.4: 44-49).

As to Claim 20, Tamarkin et al. discloses a first means (connectors 18 on the lower surface of package 13a) coupling a packaged IC 13a to a printed circuit board 12; a second means (connectors 20 on the upper surface of package 13a) for directly electrically coupling the packaged IC 13a to a second packaged IC 13b without coupling through a printed circuit board (Fig. 1).

As to Claim 22, Tamarkin et al. further discloses that the first (connectors 18) and second (connectors 20) means are located respectively on a first (lower) and second (upper) surface of the package IC 13a.

As to Claim 23, Tamarkin et al. further discloses that the second means (connectors 20 on the upper surface of package 13a) for directly electrically coupling couples standard interface signals between the first and second packaged ICs 13a and 13b (col.3: 48-58).

As to Claim 24, Tamarkin et al. discloses, in Fig. 1: an IC package 13a for an IC die 24, comprising: a first set of electrical contacts (in connectors 18 on the lower surface of package 13a) for coupling to printed circuit board 12; a connector 20

disposed on the upper surface of package 13a for coupling to a mating connector 18 on the lower surface of another IC package 13b.

As to Claim 26, Tamarkin et al. further discloses that the first set of electrical contacts (in connectors 18 on the lower surface of package 13a) and the connector 20 disposed on the upper surface of package 13b are mounted on opposite surfaces (lower and upper, as heretofore mentioned) of the IC package 13a (Fig. 1).

As to Claim 27, Tamarkin et al. further discloses that the first set of electrical contacts (in connectors 18 on the lower surface of package 13a) couple to the printed circuit board 12 through a socket 20 (Fig. 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. *Examiner's Note: Bolotin et al. is being used in the following 35 USC 103(a) rejections only for the purpose of providing a definition of a "package" in order to justify and support the Examiner's identification of the modular printed circuit boards 13a and 13b of Tamarkin et al. as the Applicant's claimed IC "packages." Thus, the following discussion under sections (i) and (ii), below, pertain to the rejections under 35 USC 103(a) of Claims 7, 8, 10-14 and 17, hereinbelow.*

(i) Bolotin et al. teaches that modular single chip or modular multi-chip printed circuit boards are considered in the art to be a "package," as shown in the exemplary Fig. 1 and described in col.1: 25-33 and col.2: 5-13. A plurality of printed circuit board (PCB) packages 242, 246 and 400 of the type shown in Fig. 1 are stacked on yet another printed circuit board, i.e., main chassis printed circuit board 200 (Fig. 2; col.2: 14-20 and 46-59). The modular PCB packages, as shown in Fig. 1, and applied as PCB packages 242, 246 and 400 in the stacked structure of Fig. 2, come in many types, such as memory, processor, or power module packages (col.1: 25-33). The application and modular structure of the PCB packages of Figs. 1 and 2 in Bolotin et al. are analogous to the PCB packages of Tamarkin et al., as relied upon for the rejections of Claims 1-6, 15, 16, 18, 20, 22-24, 26 and 27 under 35 USC § 102(e). The PCB packages 13a and 13b of Tamarkin et al. are, like those of Bolotin et al., also modular memory packages, each of whose respective packaging substrate is a printed circuit board (Tamarkin et al.: Figs. 1 and 2; col.4: 27-29) mounted on a main board 12 (col.4: 11-12 and 27-33).

(ii) Since both Bolotin et al. and Tamarkin et al. are directed to the formation of a three-dimensional electronic system comprising multi-chip modules stacked onto a main printed circuit board, and since Bolotin et al. teaches that each multi-chip module is, in fact, a "package" formed on a printed circuit board, then the multi-chip modules 13a and 13b that are formed on printed circuit boards in Tamarkin et al. are each as much a "package" as the multi-chip printed circuit board module taught in and defined as a "package" by Bolotin et al. Therefore, the Examiner is correct and justified in identifying

the multi-chip printed circuit boards 13a and 13b of Tamarkin et al. as IC "packages," analogous to the printed circuit board modules taught and defined as "packages" by Bolotin et al.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamarkin et al.--in conjunction with the "package" definition of Bolotin et al. (see section 5, above)--in view of Ikesugi et al.

I. Tamarkin et al. discloses that first and second mating connectors 18 and 20--i.e., male/female connectors (col.4: 33-37) and strongly suggests, in the package assembly of Fig. 1, that the mechanism of electro-mechanical connection between the packages 13a and 13b is "press-fit," but does not explicitly say so in the disclosure.

II. Ikesugi et al. discloses that it is old and well-known in the art of connecting circuit boards that the circuit board mating (i.e., male/female) connectors engage each other by a press-fit engagement in order to establish secure mechanical and good electrical connection therebetween (Figs. 1 and 2; col.1: 13-19)

III. Since both Tamarkin et al. and Ikesugi et al. are both in the art of electronic device packaging involving multiple circuit board assemblies using male/female board connectors, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to effect the electro-mechanical connection between the male/female mating connectors 18 and 20 in Tamarkin et al. by means of press-fit engagement, disclosed as old and well-known by Ikesugi et al. in order to easily and manually establish a reliable electro-mechanical connection between the circuit boards.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamarkin et al.--in conjunction with the "package" definition of Bolotin et al. (see section 5, above)--in view of Pecone et al.

I. Tamarkin et al. discloses that first and second mating connectors 18 and 20 are coupled to form the assembly of package substrates 13a and 13b in Fig. 1 but does not teach that first and second connectors are removably coupled.

II. Pecone et al. discloses that first (74, 76) and second (84, 86) mating connectors are removably coupled to each other (col.12: Claim 11) in order to facilitate manual assembly, replacement, repair or upgrade of the daughterboard 24 and adapter board 22.

III. Since Tamarkin et al. and Pecone et al. are both in the art of electronic device packaging and assembly wherein multiple circuit boards are assembled using mating connectors, then it would have been obvious to one ordinary skill in the art at the time the invention was made to use the removably coupled mating connectors of Pecone et al. to electro-mechanically connect the package substrates of Tamarkin et al. in order to easily disassemble the package assembly for the purpose facilitating the manual replacing, repairing, or upgrading the package substrates of Tamarkin et al. by the end user of the stacked module of Tamarkin et al.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamarkin et al.--in conjunction with the "package" definition of Bolotin et al. (see section 5, above)--in view of Miller.

I. Tamarkin et al. discloses an assembly of stacked memory packages 13a and 13b on a printed circuit board 12, the memory packages 13a and 13b having memory IC chips 24 mounted thereon (Figs. 1 and 2), wherein the first and second connectors 18 and 20, respectively, are electro-mechanically coupled to provide electrical signal connection between the memory packages 13a and 13b (col.6: 34-46), wherein the signals are dedicated (i.e., package-specific) and shared signals (i.e., for all stacked packages) to and from the ASIC on printed circuit board 12 (col.3: 48-62) and are routed over the first and second connectors, as well as over the second set of electrical contacts A, B within connector 20 on the upper right-hand-side surface of the package 13a (Figs. 1 and either of Figs. 4 or 5).

II. Tamarkin et al. does not teach, in particular, power, ground and signals of specified slower speed, relative to other signals, routed over the second set of electrical contacts A, B (within connector 20 on the upper right-hand-side surface of the package 13a in Fig. 1).

III. Miller discloses an assembly of stacked memory packages 10 on a printed circuit board 20 wherein the memory chips have power pins 11 for passing power supply and ground signals required to operate the chip, and read/write enable pins (for passing signals which are inherently slower speed signals than the faster data signals because the data signals read from or written to a chip *cycle multiple times* during *a single ON pulse of the enable signal*; thus, the data signals are faster speed signals than the read/write enable signals, or, to put it another way, *the read/write enable signals are slower speed signals than the data signals*) (Fig. 1; col.2: 50-64). The

read/write enable, power/ground, data and address signals are all routed over the electrical contacts within connectors 50 (col.3: 47-54) in order to selectively operate the memory chips as required by the system application.

IV. Since both Tamarkin et al. and Miller are both in the art of stacked IC memory packages, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include, at the very least, the chip-operational power/ground signals, the data signals and the (slower speed) read/write enable signals, taught by Miller, and as required by the system application, among the dedicated and shared signals routed over the second set of electrical contacts in Tamarkin et al. in order to selectively operate the memory chips of the memory IC packages of Tamarkin et al., as taught by Miller.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamarkin et al.--in conjunction with the "package" definition of Bolotin et al. (see section 5, above)--in view of Miremadi et al.

I. Tamarkin et al. discloses stacked first and second memory IC packages 13b and 13a,respectively, wherein the first or second ICs 24 could also be any IC or other circuit component, memory or otherwise, which benefits from the electrical and structural benefits of compact stacked packaging taught by Tamarkin et al. (col.3; 63-col.4: 7).

II. Miremadi et al. discloses stacked first and second memory IC packages 13 including ICs 23 (col.3: 61-64; col.4: 32-35) wherein the stack may be modified such that one of the corresponding first and second ICs 23 is a microprocessor for performing

computing and signal processing functions in the stacked package while the other IC 23 functions as a memory (col.4: 1-8).

III. Since Tamarkin et al. and Miremadi et al. both teach stacked IC memory packages that can have ICs that perform other functions, and since Miremadi et al. specifically teaches that one of the first and second ICs may be a microprocessor while the other IC functions as a memory in order to perform processing functions in conjunction with the memory IC, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace one of the first and second memory IC devices of Tamarkin et al. with a microprocessor to perform computational and processing functions in conjunction with the memory functions of the other IC, as taught by Miremadi et al.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamarkin et al.--in conjunction with the "package" definition of Bolotin et al. (see section 5, above)--in view of Khosrowpour et al.

I. Tamarkin et al. discloses the first set of electrical contacts A, B in connectors 20 as "internal contacts" (Figs. 4 or 5; col.5: 20-23) but does not explicitly identify their type.

II. Khosrowpour et al. discloses a first set of mating contacts in the connectors 102 of IC package 120 as, *inter alia*, pins for removable mating to another IC package 130 (Figs. 2 and 3; col.59-col.4: 15).

III. Since both Tamarkin et al. and Khosrowpour et al. interconnect IC packages using sets of electrical contacts in connectors, it would have been obvious to one of

ordinary skill in the art at the time the invention was made to use pins as the first set of electrical contacts A, B in connectors 20 for establishing removable connection to another IC package "13c" in Tamarkin et al., as taught by Khosrowpour et al.

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamarkin et al.--in conjunction with the "package" definition of Bolotin et al. (see section 5, above)--in view of Mostafazadeh et al.

I. Tamarkin et al. discloses stacked first and second memory IC packages 13b and 13a, respectively, wherein the first or second ICs 24 could also be any IC or other circuit component, memory or otherwise, which benefits from the electrical and structural benefits of compact stacked packaging (col.3: 63-col.4: 7) but does not teach the first and second connectors carry signals for a standard microprocessor interface between the first and second ICs.

II. Mostafazadeh et al. discloses stacked IC packages including memory packages and a standard (conventional) microprocessor for performing computational and processing functions in conjunction with the other IC packages in the stacked assembly, and furthermore discloses a standard microprocessor interface to interface the microprocessor package with one of the other standardized packages 32 (which include IC memory packages) wherein the microprocessor IC package may be placed at the top, bottom or middle of the IC package stack (col.5: 47-51; col.5: 60-col.6: 6; col.6: 12-15) and the connectors (balls 42) carry signals for the standard microprocessor interface (package) between the IC microprocessor and memory packages.

III. Since Tamarkin et al. and Mostafazadeh et al. both teach stacked IC packages that can have ICs that perform other functions, and since Mostafazadeh et al. specifically teaches that one of the IC packages may be a standard microprocessor requiring a standard microprocessor interface (package) between the IC microprocessor package and an IC memory package wherein the signals pass through the package connectors connecting the microprocessor IC package and the memory IC package, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the stacked IC packages in the assembly of Tamarkin et al. such that one of the first and second ICs (corresponding to the first and second IC packages) is a microprocessor, the other IC is a memory, and the first and second connectors 18 and 20 carry signals for a standard microprocessor interface (which is another IC package in the stacked assembly) between the first and second ICs in order to enable the exchange of information between the microprocessor IC and the memory IC, as taught by Mostafazadeh et al.

12. Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamarkin et al.--in conjunction with the "package" definition of Bolotin et al. (see section 5, above)--in view of Ito et al.

As to Claims 14 and 17:

I. Tamarkin et al. discloses that the first and second connectors 18 and 20, respectively, are engaged as male/female connectors (col.4: 33-37 and 44-49) but does not teach that they are slidably engaged.

II. Ito et al. discloses first and second connectors 1 (female) and 2 (male) (col.1: 26-28; col.3: 38-46) for connecting circuit boards 17 and 27, wherein the connectors 1 and 2 are slidably engaged (Figs. 1 and 2) for the purpose of facilitating registration and mating of the connectors (col.2: 41-59). [*Examiner's Note*: The reference numbers of the drawings often do not properly correspond to the reference numbers in the Specification. Therefore, to facilitate easy identification, the Examiner uses the reference numbers *in the drawings* to identify the elements described in the Specification].

III. Since Tamarkin et al. and Ito et al. both connect circuit substrates with male/female connectors, then the solution of the problem of registration and mating of the connectors taught by Ito et al. would have been readily recognized in the pertinent art of Tamarkin et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the first and second male/female connector structures of Tamarkin et al. with the slidable engagement connector structures taught by Ito et al., thus enabling a slidable engagement of the first and second connectors of Tamarkin et al. in order to facilitate the proper registration and mating of the first and second connectors taught by Ito et al.

Allowable Subject Matter

13. Claims 9, 19, 21, 25, 28 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 9, patentability resides in *high speed signals routed over the first and second connectors and power, ground and slower speed signals routed over the first set of electrical contacts*, in combination with the other limitations of the claim.

As to Claim 19, patentability resides in *sending high speed signals over the first package connector and sending lower speed signals over the first set of electrical connectors*, in combination with the other limitations of the claim.

As to Claim 21, patentability resides in *the first and second means located on a first surface of the packaged integrated circuit*, in combination with the other limitations of the claim.

As to Claim 25, patentability resides in *the first set of electrical contacts and the connector mounted on a bottom surface of the integrated circuit package*, in combination with the other limitations of the claim.

As to Claim 28, patentability resides in *high speed signals routed over the second means and power, ground and slower speed signals routed over the first means*, in combination with the other limitations of the claim.

As to Claim 29, patentability resides in *high speed signals routed over the connector and power, ground and slower speed signals routed over the first set of electrical contacts*, in combination with the other limitations of the claim.

15. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Response to Arguments

16. Applicant's arguments filed March 26, 2003 have been fully considered but they are not persuasive.

17. The Examiner's rejections of the previous Office Action of February 10, 2003 have been repeated with Bolotin et al. serving only to support, by definition of an IC "package," the Examiner's assertion that the IC printed circuit boards 13a and 13b of Tamarkin et al. are, in fact, the IC "packages" claimed by the Applicant. No new issues or grounds of rejection have been raised by the Examiner.

The Applicant traverses the 35 USC § 102(e) and 103(a) rejections of the Examiner's previous Office Action of February 10, 2003 on the basis of the argument that the elements 13a and 13b in Tamarkin et al. are printed circuit boards, as taught by Tamarkin et al., and **therefore are not the "packages" claimed by the Applicant.** The Examiner has thoroughly addressed this issue using an evidentiary reference, Bolotin et al. (US 6,206,705 B1), to prove that the multi-chip printed circuit boards 13a and 13b of Tamarkin et al. are, in fact, the "packages" of the Applicant's claimed

invention having an integrated circuit 24 mounted thereon by analogy to the single chip or multi-chip printed circuit board structures taught and defined as "packages" by Bolotin et al. (see section 3, paragraphs (ii) and (iii) of the Claim 1 rejection, and all of section 5, above, in the present Office Action). It is clear that, although Tamarkin et al. chooses to call structures 13a and 13b "printed circuit boards," they nevertheless are disclosed by Tamarkin et al. such that they meet all the structural and functional requirements for being the modular "packages" taught and defined by Bolotin et al. and therefore may be justifiably identified as, and named, "packages." As the saying goes, "looks like a *duck*, walks like a *duck*, quacks like a *duck*, swims like a *duck*..., well then, it must be a *duck*." Likewise, printed circuit boards 13a and 13b of Tamarkin et al. each have all the attributes of an IC "package," as defined by Bolotin et al., and therefore are correctly and appropriately identifiable as such.

Furthermore, a comparison of the printed circuit board chip packages 13a and 13 b of Fig. 1 of Tamarkin et al. with the Applicant's disclosed printed circuit board chip packages 103 and 110 reveals in both, functionally modular, IC-chip-carrying printed circuit boards mounted on a main printed circuit board (main PCB 12 in Tamarkin et al., and main PCB 109 in Applicant's disclosure). Structurally and functionally, both teach modular printed circuit board IC "packages" mounted on a main printed circuit board. The breadth and scope of the Applicant's claims requires no more than what Tamarkin et al., in conjunction with the "package" definition of Bolotin et al., already discloses about IC packages.

Finally, in the matter of an additional argument by the Applicant regarding the Examiner's rejection of Claim 20 (see Applicant's remarks in the above-cited instant amended Response: the last paragraph of p.3), i.e., alleging that "Tamarkin fails to disclose at least a second means for directly electrically coupling a packaged integrated circuit to a second package integrated circuit **without coupling through the printed circuit board**" (bold emphasis added), the Examiner respectfully disagrees: As indicated by the Examiner in the 35 USC § 102(e) rejection of Claim 20, above, over Tamarkin et al., Claim 20 requires a second means (connectors 20 on the upper surface of package 13a of Tamarkin et al.) for **directly** electrically coupling the packaged IC (13a in Tamarkin et al.) to a second packaged IC (13b in Tamarkin et al.) **without coupling through the printed circuit board**; i.e., the printed circuit board 12 does not interpose or intervene physically or electrically between packaged IC 13a and second packaged IC 13b; rather, packaged IC 13a is clearly disclosed by Tamarkin et al., in Fig. 1, as **directly** coupled to second packaged IC 13b, the coupling mechanism being connectors 20 (the claimed "second means for directly electrically coupling..."), **without** any physical interposition or electrical intervention by the printed circuit board 12. Thus, Tamarkin et al. teaches, in Fig. 1, exactly what Claim 20, as recited, requires and nothing less.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references disclose various printed circuit boards defined in the art as "packages" by virtue of their structure and functional applications:

Kane et al. (US 5,252,857): col.2 : 64-68 and col.3 : 46-48.

Samaras et al. (US 5,991,161): Figs. 1 and 2; col.3: 26-31.

Yasuho et al. (US 5,346,402): Fig. 1; col.4: 18-29.

Venkateshwaran et al. (US 6,339,254 B1): Fig. 6A; col.5: 57-63.

Armezzani et al. (US 6,574,113 B2): col.2: 1-16.

Degani et al. (US 2002/0079568 A1): paragraph [0070], pp.4-5.

Degani et al. (US 5,990,564): col.3: 9-10 and 16-33.

Lin et al. (US 2003/0122240 A1): paragraph [0026], pp.1-2.

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Primary Examiner
Art Unit 2827

jbv
August 4, 2003